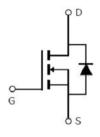


V <sub>DSS</sub>	100V		
R <sub>DS</sub> (on)	4.2m (typ.)		
I <sub>D</sub>	140A		





- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150 operating temperature



It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Symbol	Parameter	Max.	Units	
In @ Tc = 25°C	Continuous Drain Current, Vgs @ 10V	140		
In @ Tc = 100°C	Continuous Drain Current, Vos @ 10V	85	Α	
Ірм	Pulsed Drain Current	417		
Pp @Tc = 25°C	PD @Tc = 25°C Power Dissipation			
VDS	/ps Drain-Source Voltage		V	
V <sub>GS</sub> Gate-to-Source Voltage		± 20	V	
Eas	Single Pulse Avalanche Energy @ L=0.5mH	473	mJ	
las	Avalanche Current	52	Α	
TJ Tsтg	Operating Junction and Storage Temperature Range	-55 to +150	°C	

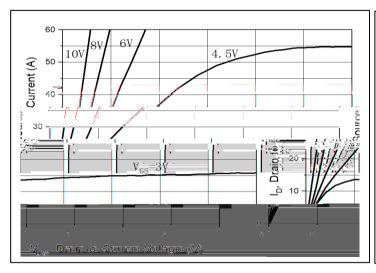


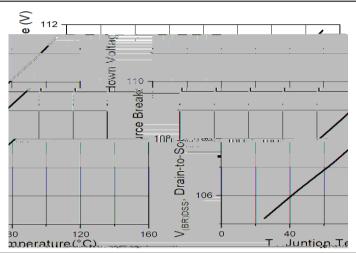
Symbol	Characterizes	Тур.	Max.	Units
R JC	Junction-to-case	_	0.47	/W
R JA	Thermal Resistance, Junction-to-Ambient	_	62	/W

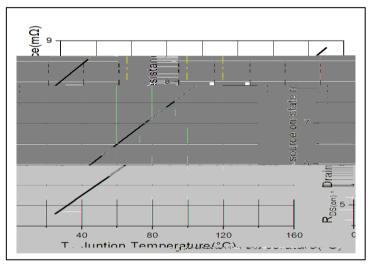
# @T<sub>A</sub>=25 unless otherwise specified

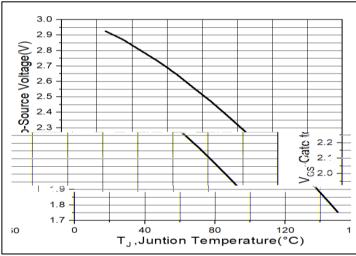
Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
V(BR)DSS	Drain-to-Source breakdown voltage	100	_	_	V	Vgs = 0V, ID = 250µA
RDS(on)	Static Drain-to-Source on-resistance	_	4.2	6	m	Vgs=10V,ID =20A
VGS(th)	Gate threshold voltage	2	_	4	V	Vps = Vgs, Ip =250µA
IDSS	Drain-to-Source leakage current	_	_	1	μA	Vps =100V,Vgs = 0V
l	Coto to Course forward lockers	_	_	100	- A	Vgs =20V
lgss	Gate-to-Source forward leakage	_	_	-100	nA	Vgs = -20V
Qg	Total gate charge	_	43	_		ID = 20A,
Qgs	Gate-to-Source charge	_	9.5	_	nC	VDS=50V,
Qad	Gate-to-Drain("Miller") charge	_	11	•	•	Vgs = 10V

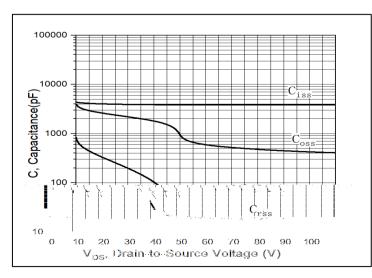
# **Typical Electrical and Thermal Characteristics**













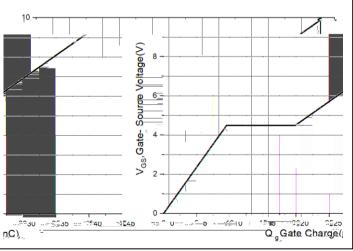
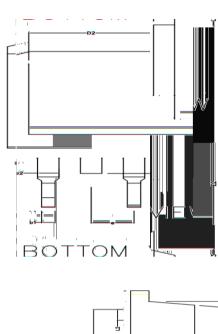


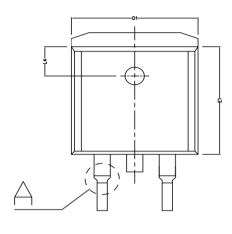
Figure6. Gate Charge

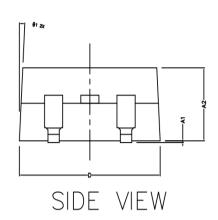




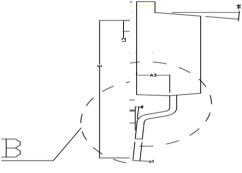
## Option 2

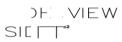


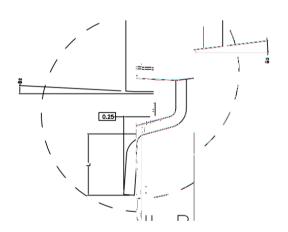




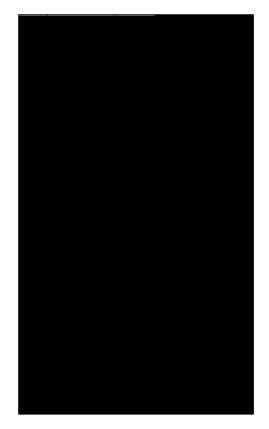
TOP VIEW













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